

AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor device comprising:

 a semiconductor substrate;

 an element isolating region having a trench formed in said semiconductor substrate and an embedding insulating film which is embedded into said trench;

 an active region formed adjacent to said element isolating region and including a well region in which a gate insulating film is formed thereon and a gate electrode is formed on the gate insulating film, wherein said well region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

 a region formed in such a manner that at least a portion of the gate electrode is positioned on said element isolating region, and a first edge surface of an upper side of said embedding insulating film in a first element isolating region portion where said gate electrode is positioned is at a vertically higher plane than a second edge surface of said embedding insulating film in a second element isolating region portion where said gate electrode is not positioned, wherein the plane of said second edge surface of said embedding insulating film is positioned at a depth, extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of said source and drain diffusion regions near the source and drain diffusion regions where an impurity concentration is greater than an impurity concentration of said well region.

2. (Currently amended) A semiconductor device as claimed in claim 1 wherein:
a height difference between said first edge surface and said second edge surface is larger than a thickness of said gate insulating film.
3. (Currently amended) A semiconductor device as claimed in claim 1 wherein:
a height difference between said first edge surface and said second edge surface is larger than a distance defined from a surface of said semiconductor substrate ~~up to a depth in to where said ion implanted source and drain regions extend impurity region where concentration of said impurity becomes maximum.~~
4. (Previously presented) A semiconductor device as claimed in claim 1 wherein:
a height difference between said first edge surface and said second edge surface is larger than, or equal to 40 nm.
5. (Previously presented) A semiconductor device as claimed in claim 1 wherein:
a height difference between said first edge surface and said second edge surface is smaller than, or equal to 200 nm.
6. (Currently amended) A semiconductor device comprising:
a semiconductor substrate;
an active region having a gate electrode formed above said semiconductor substrate and including a well region, wherein said well region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

an element isolating region having both a trench formed in said semiconductor substrate and an embedding insulating film embedded in said trench; wherein a boundary plane which is between said embedding insulating film in said element isolating region and a film deposited on said embedding insulating film and which is located at a position furthest from a bottom portion of said trench is formed at a height position lower than a surface of said semiconductor substrate where said gate electrode is formed, and wherein the lower plane surface of the embedding insulating film is positioned at a depth, extended from said surface of said semiconductor substrate, substantially the same as or greater than that of said source and drain diffusion regions near the source and drain diffusion regions where impurity concentration is greater than an impurity concentration of said well region.

7. (Currently Amended) A semiconductor device comprising:

 a semiconductor substrate;
 an active region having a gate electrode formed above said semiconductor substrate and including a well region, wherein said well region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and
 an element isolating region having both a trench formed in said semiconductor substrate and an embedding insulating film embedded in said trench; wherein a boundary plane between said embedding insulating film in said element isolating region and a film deposited on said embedding insulating film is formed at a height position lower than a surface of said semiconductor substrate where said gate electrode is formed;

wherein said active region owns an impurity region in which an impurity has been implanted into the semiconductor substrate in correspondence with said gate electrode; and

wherein a height difference between the boundary plane of said embedding insulating film and the surface of said semiconductor substrate is substantially the same as or larger than a height distance defined from the surface of said semiconductor substrate up to a depth in said impurity region to where said source and drain diffusion regions extend ~~concentration of said impurity becomes maximum.~~

8. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;
an element isolating region having a trench formed in said semiconductor substrate and an embedding insulating film embedded in said trench;
an active region formed adjacent to said element isolating region and including a well region in which a gate insulating film is formed thereon and a gate electrode is formed on said gate insulating film, wherein said well region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

an interlayer insulating film deposited on both said element isolating region and said active region, having an upper edge surface located above said gate electrode;

wherein a portion of said gate electrode is located in said element isolating region; and

wherein a portion of said interlayer insulating film which is deposited on said

element isolating region and located at a peripheral portion of said gate electrode forms a boundary plane with the embedding insulating film within the trench that is recessed from an upper plane of said embedding insulating film in said element isolating region located under said gate electrode, wherein the recessed boundary plane is at a depth, extended from a surface plane of said semiconductor substrate where said gate electrode is formed, substantially the same as or greater than that of said source and drain regions near the source and drain diffusion regions where impurity concentration is greater than an impurity concentration of said well region.

9. (Original) A semiconductor device as claimed in claim 1 wherein:

an embedding oxide film contains an HDP film which is manufactured by using plasma, the concentration of which is selected to be 1E10 to 1E12 atom/cm³.

10. (Currently amended) A semiconductor device comprising:

a semiconductor substrate;
an element isolating region having a trench formed in said semiconductor substrate and an embedding insulating film embedded in said trench;
an active region formed adjacent to said element isolating region and including a well region in which a gate insulating film is formed thereon and a gate electrode is formed on said gate insulating film, wherein said well region has ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

an interlayer insulating film deposited on both said element isolating region and said active region, having an upper edge surface located above said gate

electrode;

wherein a portion of said gate electrode is located on said element isolating region; and

wherein as to boundary planes at locations where a film is deposited on said embedding insulating film in said element isolating region, a first boundary plane in a first element isolating region portion where said gate electrode is positioned is formed at a height position higher than a second boundary plane in a second element isolating region portion located peripherally to said first element isolating region portion, the difference in height being substantially the same as or greater than the vertical extension of said source and drain diffusion regions into said semiconductor substrate; and also, said semiconductor device includes a region arranged in such a manner that a surface of said semiconductor substrate in a region where said gate electrode is arranged is positioned between said first boundary plane and said second boundary plane.

11. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate including a plurality of active regions where elements are formed in a well region, and an element isolating region for mutually isolating said plural active regions from each other;

a gate electrode formed via a gate insulating film on a surface of the active region of said semiconductor substrate, wherein each element of an active region having ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

a trench formed in the element isolating region of said semiconductor substrate, into which an embedding insulating film is embedded;

wherein an upper edge of said embedding insulating film in said trench is recessed from a surface of said active region of said semiconductor substrate towards the side of a trench bottom portion, the recessed upper edge is positioned at a depth, extended from a surface plane of said semiconductor substrate where said gate electrode is formed, substantially the same as or greater than that of said source and drain regions near the source and drain diffusion regions where impurity concentration is greater than an impurity concentration of said well region.

12. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

 a step in which a trench is formed in a semiconductor substrate, an embedding insulating film having a lower conductivity than a conductivity of said semiconductor substrate is embedded into said trench, and an element isolating region and an active region located adjacent to said element isolating region are formed;

 a step in which a gate insulating film and a gate electrode film are deposited on said semiconductor substrate, on which an insulating film is deposited and patterned so as to form a gate electrode; and

 a step in which a portion of said embedding insulating film of said element isolating region is removed, a first region where said gate electrode is positioned is formed on a surface of said embedding insulating film, and a second region lower than said first region is formed around said first region.

13. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 12 wherein:

 said embedding insulating film of said second region is removed by a

value larger than, or equal to a thickness of said gate insulating film.

14. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 12 wherein:

 said embedding insulating film of said second region is removed by a value larger than, or equal to 40 nm.

15. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 12 wherein:

 said embedding insulating film of said second region is removed by a value smaller than, or equal to 200 nm.

16. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

 a step in which a trench is formed in a semiconductor substrate, an embedding insulating film having a lower conductivity than a conductivity of said semiconductor substrate is embedded into said trench, and an element isolating region and an active region located adjacent to said element isolating region are formed;

 a step in which a gate insulating film and a gate electrode film are deposited on said semiconductor substrate, on which an insulating film is deposited and patterned so as to form a gate electrode;

 a step in which a resist is coated on the semiconductor substrate, and the coated resist is patterned; the resist is left in a first region where said gate electrode is positioned in said element isolating region; the resist of a second region where said gate electrode is not positioned is removed; and a portion of said

embedding insulating film of said second region is removed;

 a step in which a thermal oxide film is formed on a surface of said semiconductor substrate; an impurity is implanted into said semiconductor substrate by penetrating said thermal oxide film; and then, the impurity-implanted semiconductor substrate is annealed so as to form an impurity region;

 a step in which an insulating film having a lower conductivity than a conductivity of said semiconductor substrate is deposited on said semiconductor substrate;

 a step in which a hole is pierced at a position of said impurity region in said deposited insulating film so as to form a contact hole; and

 a step in which a conductive material having a higher conductivity than a conductivity of silicon is embedded into said contact hole so as to form a plug.

17. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 16 wherein:

 said embedding insulating film of the second region is removed by such a value larger than, or equal to a depth defined from the substrate in said impurity region up to maximum concentration of said impurity.

18. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

 (1) a step in which a trench is formed in a semiconductor substrate, an embedding oxide film is embedded into said trench, and both an element isolating region and an active region which is electrically isolated from said element isolating region are formed;

 (2) a step in which a gate oxide film, a gate electrode film, and an

insulating film are deposited on the semiconductor substrate, and then, said deposited films are patterned so as to form a gate electrode;

(3) a step in which a resist is coated on said semiconductor substrate, said coated resist is patterned, and a portion of the oxide film within said element isolating region is removed;

(4) a step in which a surface of said semiconductor substrate is thermally oxidized so as to form a thermal oxide film, an impurity is implanted from the upper portion of said thermal oxide film into said semiconductor substrate, and then, said implanted semiconductor substrate is annealed so as to form an impurity region;

(5) a step in which an interlayer insulating film is deposited on both said element isolating region and said active region;

(6) a step in which a hole is pierced in said interlayer insulating film so as to form a contact hole;

(7) a step in which a conductive material is embedded into said contact hole so as to form a plug which is electrically communicated to said impurity region; and

(8) a step in which a wiring layer which is electrically communicated to said plug is formed on said interlayer insulating film.

19. (Previously Presented) A method of manufacturing a semiconductor device comprising:

a step for forming an oxide film on a semiconductor substrate;

a step for forming an oxidation preventing film on said oxide film;

a step for removing both said oxidation preventing film and said oxide

film of a predetermined region so as to expose said semiconductor substrate;

 a step for etching said exposed substrate so as to form a trench;

 a step for depositing an insulating film on both said trench and said oxidation preventing film;

 a step for removing said insulating film deposited on said oxidation preventing film;

 a step for forming a plurality of element isolating trenches into which said deposited element is formed;

 a gate electrode formed via a gate insulating film on a surface of an active region of the semiconductor substrate; and

 a trench formed in said element isolating region of the semiconductor substrate, which is embedded by an embedding insulating film;

 wherein each element of an active region having ion implanted source and drain diffusion regions provided in correspondence to said gate electrode; and

 wherein an upper edge of the embedding insulating film in said trench is caused to become recessed from the surface of said active region towards the side of a trench bottom portion.

20. (Currently Amended) A semiconductor device comprising a plurality of element isolating portions made of an insulating film embedded into a trench on a major surface of a semiconductor substrate, wherein:

 in a first region where a width of an active region is relatively small, a recess amount of each element isolating portion corresponding thereto is relatively large, whereas in a second region where a width of an active region is relatively large, a recess amount of each element isolating portion corresponding thereto is

equal to zero, or relatively small.

21. (Currently Amended) A semiconductor device as claimed in claim 20 wherein:

the width of said active region in said first region is smaller than 1 μm , and the width of said active region in said second region is larger than, or equal to 1 μm .

22. (Currently Amended) A semiconductor device comprising: a memory array constituted by a plurality of memory cells arranged on a semiconductor substrate in a matrix shape; a peripheral circuit region where a circuit element different from said plurality of memory cells is formed; and a plurality of element isolating portions made of an insulating film embedded into a trench on a major surface of a semiconductor substrate, wherein:

in said memory array, a recess amount of each element isolating portion corresponding thereto is relatively large, whereas in said peripheral circuit region, a recess amount of each element isolating portion corresponding thereto is equal to zero, or relatively small.

23. (Currently Amended) A semiconductor device as claimed in claim 22 wherein:

the width of an active region in said memory array is smaller than 1 μm , and the width of an active region in said peripheral circuit region is larger than, or equal to 1 μm .

24. (Original) A semiconductor device as claimed in claim 22 wherein:

the recess amount of said element isolating portion in said memory

array is approximately 80 nm, whereas the recess amount of said element isolating portion in said peripheral circuit region is approximately 0 to 40 nm.

25. (Original) A semiconductor device as claimed in claim 22 wherein:

an activated region in said memory array is a stripe shape.

26. (Original) A semiconductor device as claimed in claim 22 wherein:

 said plurality of memory cells constitute memory cells of a flash memory arranged by that source/drain regions of said plurality of memory cells are mutually connected in parallel thereto in each of columns, and a plurality of word lines are elongated in each of rows.

27. (Original) A semiconductor device as claimed in claim 26 wherein:

 each of said plural memory cells is comprised of:

 a lower layer conductive film for a floating gate electrode, which is provided via a first insulating film on a channel region between said source/drain regions;

 an upper layer conductive film for a floating gate electrode, which is electrically connected to said lower layer conductive film for the floating gate electrode, and is elongated from said lower layer conductive layer for the floating gate electrode via a second insulating film formed on said source/drain region to said source/drain region; and

 a conductive film for a control gate electrode, which is provided via a third insulating film on the upper layer conductive film for the floating gate electrode, and is operated as said word line overlapped on said upper layer conductive film for

the floating gate.

28. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

(a) a step in which a first trench is formed in a first region of a semiconductor substrate, and a second trench is formed in a second region different from said first region;

(b) a step in which after an insulating film has been deposited on said substrate, said deposited insulating film is flattened so as to embed said insulating film into both said first and second trenches; and

(c) a step in which after said second region has been covered by a resist pattern, said insulating film embedded into said first trench is etched in order that an upper surface of said insulating film embedded into said first trench is caused to fall from an upper surface of said insulating film embedded into said second trench, a first element isolating portion is formed in said first region, and a second element isolating portion is formed in said second region; wherein:

 said first region is a region where a width of an activated region is relatively small, whereas said second region is a region where a width of an activated region is relatively large.

29. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 28 wherein:

 a recess amount of said first element isolating portion is relatively large, whereas a recess amount of said second element isolating portion is either zero, or relatively small.

30. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 28 wherein:

the width of said activated region in said first region is smaller than 1 μm , and the width of said activated region in said second region is larger than, or equal to 1 μm .

31. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 28, further comprising:

(d) a step in which a gate insulating film has been formed on a major surface of said substrate, a conductive film is deposited on said resulting substrate, and while a resist pattern is employed as a mask, said conductive film is treated so as to form a gate electrode made of said conductive film in said first region; and

(e) a step in which an impurity is conducted into the respective substrates on both sides of said gate electrode formed in said first region so as to form a source/drain region.

32. (Withdrawn) In a method of manufacturing a semiconductor device having a plurality of memory cells arranged in a semiconductor substrate in a matrix shape, in which each of said plural memory cells owns both a floating gate electrode and a control gate electrode; source/drain regions of said plural memory cells are mutually connected in parallel thereto in each of rows; and also both a memory cell constituted by that a word line formed with said control gate electrode in an integral body is elongated along a column direction corresponding to a gate length direction of said plural memory cells, a peripheral circuit region which is constructed of a circuit element different from said plural memory cells are formed,

said semiconductor device manufacturing method comprising:

(a) a step in which a first trench is formed in a region which constitutes an element isolating portion of said memory array of said substrate, and a second trench is formed in a region which constitutes an element isolating portion of said peripheral circuit region of said substrate;

(b) a step in which after a first insulating film has been deposited on said substrate, said first deposited insulating film is flattened so as to embed said insulating film into both said first and second trenches; and

(c) a step in which after said peripheral circuit region has been covered by a resist pattern, said first insulating film embedded into said first trench is etched in order that an upper surface of said first insulating film embedded into said first trench is caused to fall from an upper surface of said first insulating film embedded into said second trench, a first element isolating portion is formed in said memory array, and a second element isolating portion is formed in said peripheral circuit region.

33. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 32 wherein:

a recess amount of said first element isolating portion in the memory array is relatively large, whereas a recess amount of said second element isolating portion in the peripheral circuit region is either zero, or relatively small.

34. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 33 wherein:

the width of said activated region in said memory array is smaller than

1 μm , and the width of said activated region in said peripheral circuit region is larger than, or equal to 1 μm .

35. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 33 wherein:

the recess amount of said first element isolating portion in said memory array is approximately 80 nm, whereas the recess amount of said second element isolating portion in said peripheral circuit region is approximately 0 to 40 nm.

36. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 33 wherein:

an activated region in said memory array is a stripe shape.

37. (Withdrawn) A semiconductor device manufacturing method as claimed in claim 32, further comprising:

(d) a step in which a second insulating film which constitutes a gate insulating film of a field-effect transistor is formed on the activated region of said memory cell;

(e) a step in which a lower layer conductive film for a floating gate electrode is formed on said second insulating film in such a manner that said lower layer conductive film is elongated along said first direction in the activated region of said memory array;

(f) a step in which an impurity is conducted into said substrate on both sides of said under layer conductive film for the floating gate electrode so as to form a source/drain region elongated along said first direction;

(g) a step in which a third insulating film which is made thicker than said second insulating film on said source/drain region;

(h) a step in which an upper layer conductive film for a floating gate electrode, which is connected to an upper layer of said lower layer conductive film for the floating gate electrode and is elongated over said third insulating film, is formed along said first direction;

(i) a step in which a fourth insulating film is formed on an upper layer of said upper layer conductive film for the floating gate electrode;

(j) a step in which a conductive film for a control gate electrode is formed on said fourth insulating film; and

(k) a step in which said conductor film for the control gate electrode, said upper conductive film for the floating gate electrode, and said lower conductive film for the floating gate electrode are patterned along a second direction corresponding to said column direction so as to form both a word line which is formed with said control gate electrode in an integral manner, and said floating gate electrodes.

38. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

a step in which an element isolating trench is formed in a semiconductor substrate, and an embedding insulating film having a lower conductivity than a conductivity of said substrate is embedded into said element isolating trench so as to form an element isolating portion;

a step in which a gate insulating film, a gate electrode film, and an insulating film are deposited on said semiconductor substrate, and said deposited films are patterned so as to form a gate electrode;

a step in which an impurity is conducted into said semiconductor substrate located at a peripheral portion of said gate electrode;

a step in which a portion of said embedding insulating film of said element isolating portion is removed, and the highest region of said embedding insulating film is caused to be lowered than a surface of said semiconductor substrate;

a step in which said semiconductor substrate is thermally treated; and

a step in which an electrically communicating plug is formed in a region of said semiconductor substrate, into which said impurity has been conducted.

39. (Withdrawn) A method of manufacturing a semiconductor device, comprising:

a step in which an element isolating trench is formed in a semiconductor substrate, and an embedding insulating film having a lower conductivity than a conductivity of said substrate is embedded into said element isolating trench so as to form an element isolating portion;

a step in which a gate insulating film, a gate electrode film, and an insulating film are deposited on said semiconductor substrate, and said deposited films are patterned so as to form a gate electrode;

a step in which a side wall made of an insulating film is formed on a side wall of said gate electrode;

a step in which an impurity is conducted into said semiconductor substrate located at a peripheral portion of said side wall;

a step in which a portion of said embedding insulating film of said element isolating portion is removed, and the highest region of said embedding insulating film is caused to be lowered than a surface of said semiconductor

substrate;

a step in which said semiconductor substrate is thermally treated; and
a step in which a plug is formed which electrically communicates with a
region of said semiconductor substrate, into which said impurity has been
conducted, and a wiring line formed at an upper layer above said gate electrode.

40. (Previously presented) A semiconductor device as claimed in claim 20, wherein:

the active region in said first region includes a well region in which an
insulated gate electrode is formed thereon, said well region having ion implanted
source and drain diffusion regions in correspondence to said insulated gate
electrode, and

said element isolating portion of said first region is positioned near the
source and drain diffusion regions where an impurity concentration is greater than an
impurity concentration of said well region thereof.

41. (Previously presented) A semiconductor device as claimed in claim 20, wherein:

said first region includes at least one well region each including one or
more of said active region with an insulated gate formed thereon, each said active
region containing ion implanted source and drain diffusion regions in
correspondence to said insulated gate electrode thereof, and

each said element insulating portion of said first region is positioned
near the source and drain diffusion regions where an impurity concentration is
greater than an impurity concentration of said well region thereof.

42. (Previously presented) A semiconductor device according to claim 20, wherein:

a height difference of the recess amount between that of a respective element isolation portion corresponding to said first region and a respective element isolation portion corresponding to said second region is larger than a distance defined from the semiconductor substrate surface to a depth where a doping concentration of an impurity region becomes maximum in the active region of said first region.

43. (Previously presented) A semiconductor device according to claim 22, wherein:
said memory array includes at least one well region each including one or more of said active region with an insulated gate formed thereon, each said active region containing ion implanted source and drain diffusion regions in correspondence to said insulated gate electrode thereof, and
each said element insulating portion of said memory array is positioned near the source and drain diffusion regions where an impurity concentration is greater than an impurity concentration of said well region thereof.

44. (Previously presented) A semiconductor device according to claim 22, wherein:
a height difference of the recess amount between that of a respective element isolation portion corresponding to said memory array and a respective element isolation portion corresponding to said peripheral circuit region is larger than a distance defined from the semiconductor substrate surface to a depth where a doping concentration of an impurity region becomes maximum in the active region.

45. (Previously presented) A semiconductor device according to claim 1, wherein:
an upper edge surface of the insulating film embedded in at least one

of the first and second element isolating region portions faces an interlayer insulating film.

46. (Previously presented) A semiconductor device according to claim 1, wherein:

an upper edge surface of the insulating film embedded in at least one of the first and second element isolating region portions faces a film for a contact plug.

47. (Previously presented) A semiconductor device according to claim 27, wherein:

a height difference of the recess amount between that of a respective element isolation portion corresponding to said memory array and a respective element isolation portion corresponding to said peripheral circuit region is larger than a distance defined from the semiconductor substrate surface to a depth where a doping concentration of an impurity region becomes maximum in the active region.

48. (Previously presented) A semiconductor device according to claim 43, wherein:

a height difference of the recess amount between that of a respective element isolation portion corresponding to said memory array and a respective element isolation portion corresponding to said peripheral circuit region is larger than a distance defined from the semiconductor substrate surface to a depth where a doping concentration of an impurity region becomes maximum in the active region.